

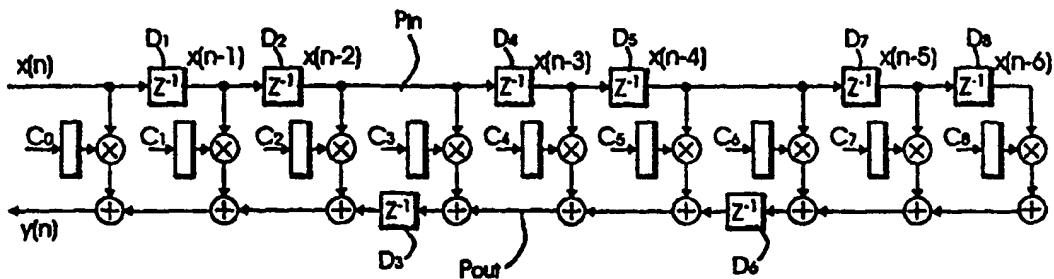


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(54) Title: FIR FILTER STRUCTURE WITH LOW LATENCY FOR GIGABIT ETHERNET APPLICATIONS



(57) Abstract

A digital filter has an input path and an output path and includes a set of delay elements and a number of taps. The taps couple the input path to the output path. Each of the taps has a coefficient, a multiplier and an adder. Each of the delay elements is disposed between two adjacent taps. The delay elements are placed in either the input path and the output path of the digital filter, such that the digital filter has fewer delay elements in the input path than a direct-form digital filter with the same number of taps in a direct-form structure, and has fewer delay elements in the output path than a transposed-form digital filter with the same number of taps in a transposed-form structure; and such that the digital filter has same transfer function as the direct-form digital filter and the transposed-form digital filter.

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INTERNATIONAL SEARCH REPORT

Int. Application No.
PCT/US 99/26483

A. CLASSIFICATION OF SUBJECT MATTER					
IPC 7 H03H17/06 H04B3/23 H04B3/32 H04L25/14 H04L25/497 H04L1/00					
According to International Patent Classification (IPC) or to both national classification and IPC					
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Category *	Citation of document, with indication, where appropriate, of the relevant passages				Relevant to claim No.
X	<p>DUNCAN ET AL.: "Strategies for design automation of high speed digital filters" JOURNAL OF VLSI SIGNAL PROCESSING, vol. 9, no. 1/2, September 1995 (1995-09), pages 105-118, XP000525889 Dordrecht, NL page 105, left-hand column, paragraph 1 page 105, right-hand column, paragraph 3 page 108, right-hand column, paragraph 2 - paragraph 4 page 108, right-hand column, paragraph 6 -page 109, left-hand column, paragraph 1 --- -/-</p>				1-20
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/26483

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
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